Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A method for designing an integrated circuit, comprising:
   receiving data specifying a plurality of interconnects and components of a design of an integrated circuit; and
   optimizing the design of the integrated circuit, wherein data specifying the plurality of interconnects and devices of the integrated circuit is optimized based on at least one of ~~bandwidth,~~ latency, scalability, [[and]] or isochronous interconnect configuration.

2. (original): The method as described in claim 1, wherein the optimized data is programmed into a self-programmable integrated circuit so as to provide the designed integrated circuit.

3. (original): The method as described in claim 1, wherein the optimized data is utilized to synthesize an integrated circuit having the specified design.

4. (currently amended): The method as described in claim 1, wherein the optimized design includes a specified characteristic for the interconnect, wherein the specified characteristic includes at least one of ~~bandwidth,~~ latency [[and]] or scalability.

5. (original): The method as described in claim 1, wherein a direct connectivity definition, derived the optimized data, is utilized to synthesize an integrated circuit.

6. (original): The method as described in claim 1, wherein optimizing includes

at least one of arranging components of the integrated circuit and specifying bandwidth between components.

7. (original): The method as described in claim 1, wherein optimizing is performed without user intervention by an agent.

8. (original): The method as described in claim 1, wherein the integrated circuit is at least one of an application specific integrated circuit (ASIC) and multiple application specific integrated circuits (ASICs).

9. (original): The method as described in claim 1, wherein interconnects not specified by a user are automatically configured by an agent.

10. (currently amended): A self-programmable integrated circuit, comprising:
a processor suitable for performing a program of instructions, the processor accessible via a first interconnect;
at least two components of the integrated circuit, the components communicatively connected via a second interconnect; and
a memory suitable for storing a program of instructions, wherein the program of instructions configures the processor to optimize the integrated circuit based on heuristic data indicating past utilization of components of the integrated circuit, wherein the heuristic data is optimized based on at least one of ~~bandwidth,~~ latency, scalability, [[and]] or isochronous interconnect configuration.

11. (currently amended): The self-programmable integrated circuit as described in claim 10, wherein the components include at least one of a core, functional block [[and]] or logical block.

12. (original): The self-programmable integrated circuit as described in claim 10, wherein the heuristic data includes data indicating amount of data transferred between a first component and a second component over the second interconnect.

13-20. (canceled)